EXAMINER'S AMENDMENT

1) An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Robert Crawford on 7/28/10.

The application has been amended as follows:

IN THE CLAIMS:

Please delete claim 10.

Please replace claim 1 with the following:

-- A method of manufacturing a semiconductor device on a region of silicon oxide situated next to a region of monocrystalline silicon at a surface of a semiconductor body, the method comprising the steps of:

1) forming a layer of arsenic on the region of monocrystalline silicon by heating the silicon oxide and monocrystalline regions in an atmosphere with an arsenic compound, the layer of arsenic not being formed on the region of silicon oxide; and, thereafter,

2) forming a layer of non-monocrystalline silicon as an auxiliary layer on the region of silicon oxide by heating the semiconductor body in an atmosphere that includes a gaseous silicon compound and that does not include a gaseous arsenic

compound, the layer of non-monocrystalline silicon not being formed on the region of monocrystalline silicon;

wherein the layer of arsenic is removed and then a silicon-containing layer is deposited on the region of monocrystalline silicon.--

Please replace claim 11 with the following:

--A method of manufacturing a semiconductor device on a region of silicon oxide situated next to a region of monocrystalline silicon at a surface of a semiconductor body, the method comprising:

1) forming a layer of arsenic on the region of monocrystalline silicon by heating the silicon oxide and monocrystalline regions in an atmosphere with an arsenic compound, the layer of arsenic not being formed on the region of silicon oxide; and, thereafter,

2) forming a layer of non-monocrystalline silicon as an auxiliary layer on the region of silicon oxide by heating the semiconductor body in an atmosphere that includes a gaseous silicon compound and that does not include a gaseous arsenic compound, the layer of non-monocrystalline silicon not being formed on the region of monocrystalline silicon, wherein the semiconductor body further includes a buried layer and a contact zone that is situated next to the region of silicon oxide at the surface of the semiconductor body, the contact zone extending from the surface of the semiconductor body to the buried layer, and wherein the layer of arsenic is also formed on the contact zone during step 1) and the layer of non-monocrystalline silicon is not formed on the contact zone during step 2).--

REASONS FOR ALLOWANCE

2) The following is an examiner's statement of reasons for allowance: Upon review of the amendments made, the closest prior art cited (Wild 698, Hamasaki 448, and Todd 825) fail to disclose or obviate a rationale for the critical limitation of independent claim 1 featuring the removal of the arsenic layer from the single crystal silicon layer followed by a deposition of a silicon containing layer ontop of the same single crystal silicon layer, after arsenic removal.

With respect to now independent claim 11 none of the prior art cites the methodology for formation that includes or obviate the steps of "...the semiconductor body further includes a buried layer and a contact zone that is situated next to the region of silicon oxide at the surface of the semiconductor body, the contact zone extending from the surface of the semiconductor body to the buried layer, and wherein the layer of arsenic is also formed on the contact zone during step 1) and the layer of non-monocrystalline silicon is not formed on the contact zone during step 2)".

Thus it is the examiner's position that the claimed invention has met the conditions for patentability. For further information please refer to applicant's remarks.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to G. NAGESH RAO whose telephone number is (571)272-2946. The examiner can normally be reached on 8:30AM-5PM (INDEPENDENT FLEX SCHEDULE).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael KORNAKOV can be reached on (571)272-1303. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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